REMARKS

This is a full and timely response to the non-final Office Action mailed on May 21, 2003. Reexamination and reconsideration in light of the following remarks are courteously requested.

Claims 3, 5-7, 11, 13-20, 23-29, 31, 37, 43-48 are currently pending in this application, with claims 3 and 25 being independent.

No new matter has been added.

Rejection Under 35 U.S.C. §102

Claims 3, 5-7, 11, 13-20, 23-29, 31, 37, 43-48 were rejected under 35 U.S.C. 102 as allegedly being anticipated by U.S. Patent 4,825,203 issued to Takeda et al. (Takeda).

These rejections are respectfully traversed for at least the following reasons.

Claim 3 and the claims dependent thereon

Within the claims, the total number of signal lines is different than the number (n) of output terminals of each of the plurality of driver circuits.

Regarding the use of Takeda, calculations provided within the Office Action arguably teach the total number of signal lines in Takeda being ***the same as*** the number (n) of output terminals of each of the plurality of driver circuits.

However, the claimed invention provides that the total number of signal lines ***is different than*** the number (n) of output terminals of each of the plurality of driver circuits.

Thus, all claimed features are not found within Takeda.

Claim 25 and the claims dependent thereon

The Office Action contends that figure 1(A) of Takeda teaches at least one general driver circuit q_1 and q_2, and further contends that at least one general driver circuit q_1 and q_2 has a quantity of 5 signal lines. In this regard, 5 signal lines ***ARE NOT SHOWN*** as the signal lines for circuits q_1 and q_2 of figure 1(A). Instead, figure 1(A) arguably depicts a **single output** Q1 corresponding to a **single circuit** q_1 and a **single output** Q2 corresponding to a **single circuit** q_2.

Within the claims, however, each at least one general driver circuit has a ***plurality of general driver circuit output***

terminals, wherein a general driver circuit output terminal of the plurality of general driver circuit output terminals provide a signal potential to one of the plurality of signal lines. But please note that a driver circuit q_N shown within figure 1(A) of Takeda corresponds only to ***a single output QN***.

Moreover, the Office Action contends that circuit q_N shown within figure 1(A) of Takeda is a remainder driver circuit, while also contending that the remainder driver circuit has 2 output terminals.

In response to this contention, figure 1(A) reveals that circuit q_N has only a single output QN, and not 2 outputs as contended within the Office Action.

In addition, Takeda arguably teaches at least one general driver circuit 13 (figure 2, column 3, lines 4-7), but fails to depict a remainder driver circuit. Instead, figure 1(A) of Takeda, which has been relied upon within the Office Action, is merely a depiction of the general driver circuit 13 (column 2, lines 23-28).

Thus, all claimed features are not found within Takeda.

Conclusion

For the foregoing reasons, all the claims now pending in the present application are believed to be clearly patentable over the prior art of record. Accordingly, favorable reconsideration of the newly presented claims in light of the above remarks is courteously solicited.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Respectfully submitted,

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